AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of claims:

1. (CURRENTLY AMENDED) A test method comprising:

a) providing a first, second and third test structure each having a respective first, second and third test structure parameter;

b) obtaining from each of the first, second and third test structure at least one test measurement value, ~~values on a device at one or more independent variable values~~ the test measurement values varying based on the first, second and third test structure parameter;

c) ~~b)~~ calculating a goodness of fit value for a fitted curve between :

(1) said test measurement values; and

(2) ~~the independent variable~~ values of the first, second and third test structure parameter;

d) ~~c)~~ using said goodness of fit value to monitor ~~the~~ processes used to form ~~said~~ a device.

2. (CURRENTLY AMENDED) The method of claim 1 wherein step d) ~~(c)~~ further includes using control limits on the goodness of fit value and using said goodness of fit value to: (1) control the processes used to form the device or (2) screen the ~~devices~~ device.

3. (CURRENTLY AMENDED) The method of claim 1 wherein step d) ~~(c)~~ further includes using control limits on the goodness of fit value; said control limits established based on a history of goodness of fit values or on device requirements; and using said goodness of fit value to: (1) control the processes used to form the device or (2) screen the ~~devices~~ device.

4. (PREVIOUSLY PRESENTED) The method of claim 1 wherein the goodness of fit value is a correlation coefficient or a standard error measurement.

5. (ORIGINAL) The method of claim 1 wherein the fitted curve is a least squares fitted straight line.

6. (CURRENTLY AMENDED) The method of claim 1 wherein the test measurement values are resistance or capacitance measurements values; and step d) ~~(c)~~ further comprises ~~and~~ using said goodness of fit value to: (1) control the processes used to form the device or (2) screen the ~~devices~~ device.

7. (CURRENTLY AMENDED) A test method comprising:

a) providing a device structure that has at least a first test structure, a second test structure and a third test structure incorporating [[a]] resistive portions ~~portion~~ from which resistance is measured;

(1) said resistive portions ~~portion~~ having an effective length (Lx) and an effective width (Wx),

(2) said first, second and third test structures have resistive portions with different effective widths (W1 W2, ... Wi);

(3) said resistive portions ~~portion~~ of said first, second and third ~~type~~ test structures have effective lengths (L1, L2, .. Li);

b) measuring the resistance (R) of the test structures;

c) calculating a goodness of fit value for a fitted curve between:
(1) said effective lengths ~~length~~ divided by the measured resistances ~~resistance~~ (L1/R1, L2/R2, ..Li /Ri); and
(2) the effective widths (W1, W2, ..Wi) of the resistive portions of the test structures;

d) using said goodness of fit value to: (1) control ~~the~~ processes used to form the device structure or (2) screen the ~~devices~~ device structure.

8. (ORIGINAL) The method of claim 7 wherein said fitted curve is a fitted straight line fitted using a least squares method.

9. (ORIGINAL) The method of claim 7 wherein said test structures are formed in and/or over a wafer.

10. (ORIGINAL) The method of claim 7 wherein said test structures are comprised of a doped region in a wafer.

11. (CANCELED)

12. (ORIGINAL) The method of claim 7 wherein said test structures are comprised of a conductive material and an interconnect layer in a semiconductor device is comprised of said conductive material.

13. (ORIGINAL) The method of claim 7 wherein said test structures are comprised of metal from a metal layer that is used to form metal lines in a semiconductor device.

14. (ORIGINAL) The method of claim 7 wherein said test structures are comprised of a material selected from the group consisting of silicon, amorphous silicon, polysilicon, polycide, silicide, metal, copper, aluminum, and alloys and combinations thereof.

15. (ORIGINAL) The method of claim 7 wherein said goodness of fit value is a correlation coefficient, coefficient of determination or standard error measurement test.

16. (CURRENTLY AMENDED) The method of claim 7 wherein said resistive portions have said effective lengths ~~length~~ being substantially greater than said effective widths ~~width,~~ and said effective widths ~~width~~ being selected to be substantially greater than an expected critical dimension loss for said ~~process~~ processes.

17. (CURRENTLY AMENDED) The method of claim 7 wherein the measuring the resistance (R) of the test structures [[;]] comprises measuring the resistance at different temperatures; and

further includes : calculating the goodness of fit value for a straight line for the between:

(1) the effective lengths ~~length~~ divided by the measured resistances ~~resistance~~ (L1/R1, L2/R2, ..Li /Ri).; the effective lengths ~~length~~ of the test structures ~~structure~~ are equal (L1 = L2 =.. Li); and

(2) the effective widths (W1, W2, ..Wi) of the test structures; and

(3) the temperature.

18. (CURRENTLY AMENDED) The method of claim 7 wherein said device structure is a wafer; said wafer has at least three test structures;

the goodness of fit value ~~measurement~~ is calculated on measurements made on the test sites on said wafer.

19. (CURRENTLY AMENDED) The method of claim 7 wherein said device structure is a printed circuit board, a ceramic substrate or a chip scale package.

20. (CURRENTLY AMENDED) The method of claim 7 wherein structures are formed adjacent to said resistive portion to measure ~~the~~ effects of micro loading or chemical-mechanical polishing. [[,]]

21. (CURRENTLY AMENDED) A method for estimating defect levels by ~~goodness of fit~~ measurements related to resistance of an interconnect layer in a process for manufacturing an integrated circuit, said method comprising the steps of:

a) fabricating on a wafer, using processes ~~said manufacturing process,~~ at least a first test structure, a second test structure and a third ~~type~~ test structure incorporating a resistive portion from which a resistance is measured;[[,]]

b) said resistive portion having an effective length and an effective width, said effective length being substantially greater than said effective width, and said effective width being selected to be substantially greater than an expected critical dimension loss for said processes ~~process~~;

c) measuring said resistance of the test structures; and

d) deriving the sheet resistances ~~resistance~~ from the resistance measurements ~~measurement~~;

e) calculating a goodness of fit value between the one divided by the sheet resistances ~~resistance~~ (1/Rs) and a second parameter;

f) using said goodness of fit value to: (1) control the processes used to form the test structures or (2) screen the test structures.

22. (ORIGINAL) The method of claim 21 where said second parameter is the effective width of the test structures or the temperature.

23. (CURRENTLY AMENDED) A test method comprising:

a) providing a device structure that has at least a first test structure, a second test structure and a third test structure from which a test parameter is measured;

b) measuring ~~the~~ test parameter values on the test structures;

c) calculating a goodness of fit value for a fitted curve between :

(1) the test parameter values and

(2) a dimensional measurement of the test structures;

d) using said goodness of fit value to: (1) control the processes used to form the device structure ~~structures~~ or (2) screen the device structure ~~structures~~.

24. (ORIGINAL) The method of claim 23 wherein said test parameter is resistance or capacitance.

25. (CURRENTLY AMENDED) A test method comprising:

a) providing a device structure that has at least a first test structure,

b) measuring a first test measurement, a second test measurement and a third test measurement on at least the first test structure;

c) calculating a goodness of fit value for a fitted curve between at least:

(1) [[a]] the first test measurement performed under a first test condition and

(2) [[a]] the second test measurement performed under a second test condition;

(3) [[a]] the third test measurement performed under a third test condition;

d) using said goodness of fit value to: (1) control ~~the~~ processes used to form the device structure or (2) screen the ~~devices~~ device structure.

26. (PREVIOUSLY PRESENTED) The method of claim 25 wherein: said first test condition, said second test condition and said third test condition are different temperatures.

27. (CURRENTLY AMENDED) The method of claim 25 wherein:

said first test structure is a resistance test structure that has a effective length (L) and effective Width (W);

said first test condition, said second test condition, and said third test

condition ~~conditions~~ have different temperatures;

said first test measurement is a resistance test measurement;

said goodness of fit value ~~measurement~~ is for a straight line fitted to (1) the effective length (L) divided by the resistance (R) vs (2) the effective width (W).

28. (CANCELED)

29. (CANCELED)

30. (CURRENTLY AMENDED) The method of claim 1 wherein the test measurement values are obtained on two or more test sites on the device.

31. (CURRENTLY AMENDED) The method of claim 1 wherein the test measurement values are obtained at two of more test conditions on the device.

32. (NEW) The method of claim 1 wherein the first, second and third test structure parameter comprises at least one of length or width of a resistive portion of the respective first, second and third test structure.

33. (NEW) The method of claim 1 wherein the first, second and third test structure parameter comprises an area of a capacitive portion of the respective first, second and third test structure.

34. (NEW) The method of claim 1 wherein the test measurement values comprises resistance or capacitance.